

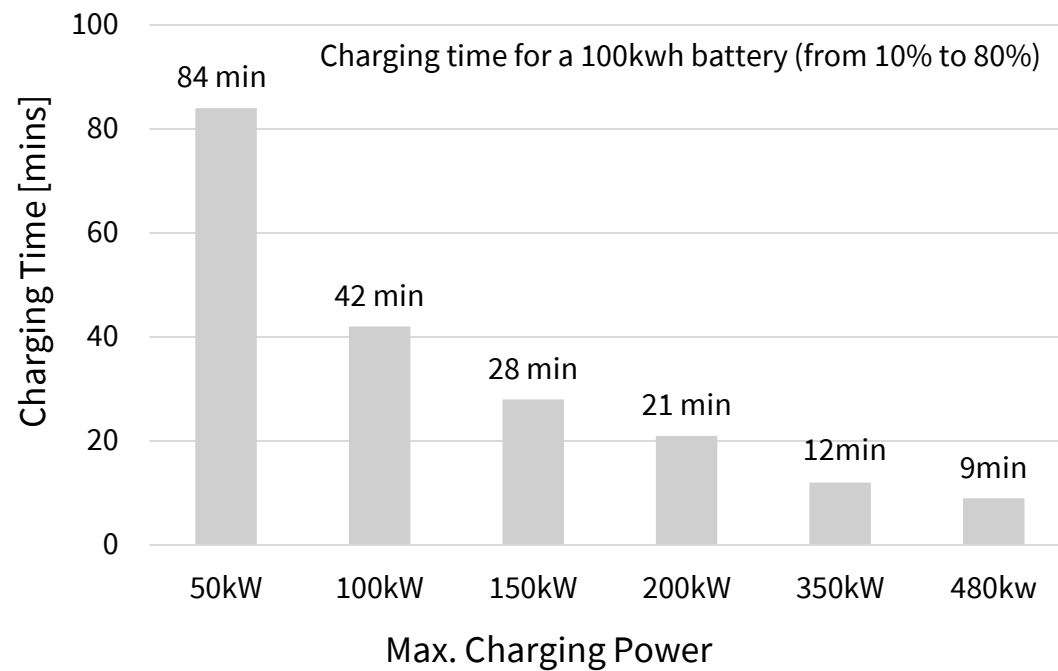
# **CRD-60DD12N-K - 60kW Three Phases Interleaved LLC Converter for EV Fast Charger**



# TREND FOR EV DC FAST CHARGING: INCREASED POWER AND VOLTAGE

## • Charging Power vs. Charging Time

- Max. Charging Power for Selected EV from Major Automakers



≥400kW  
800V



E-bus



Cargo truck



Semi-truck



Heavy duty



EVTOL

350kW  
800V



Porsche  
Taycan



Audi  
E-tron GT



Hyundai  
Ioniq 5



Aston Martin  
Rapide E



Fisker  
EMotion

250kW  
400V



Tesla Model 3



Tesla Roadster



Tesla Cybertruck

200kW  
400V



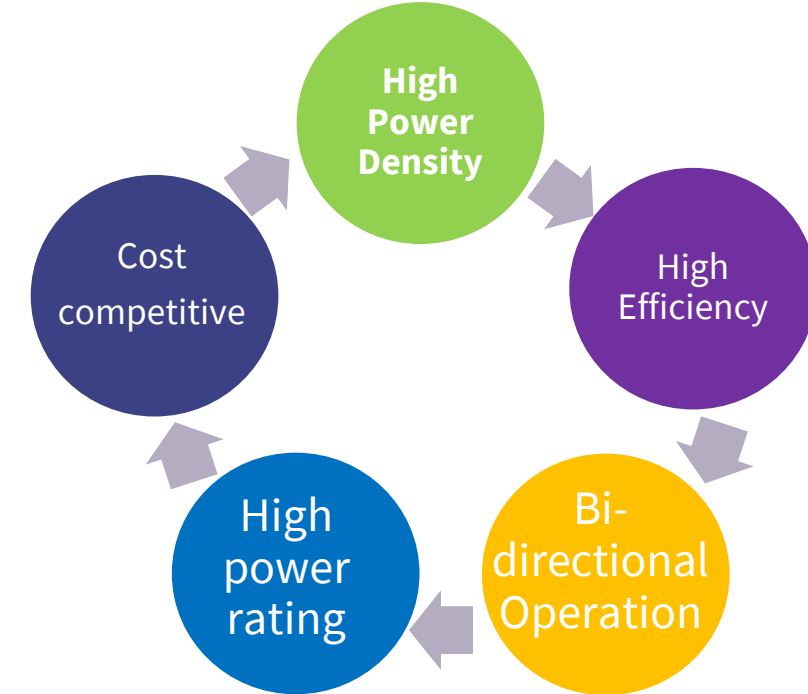
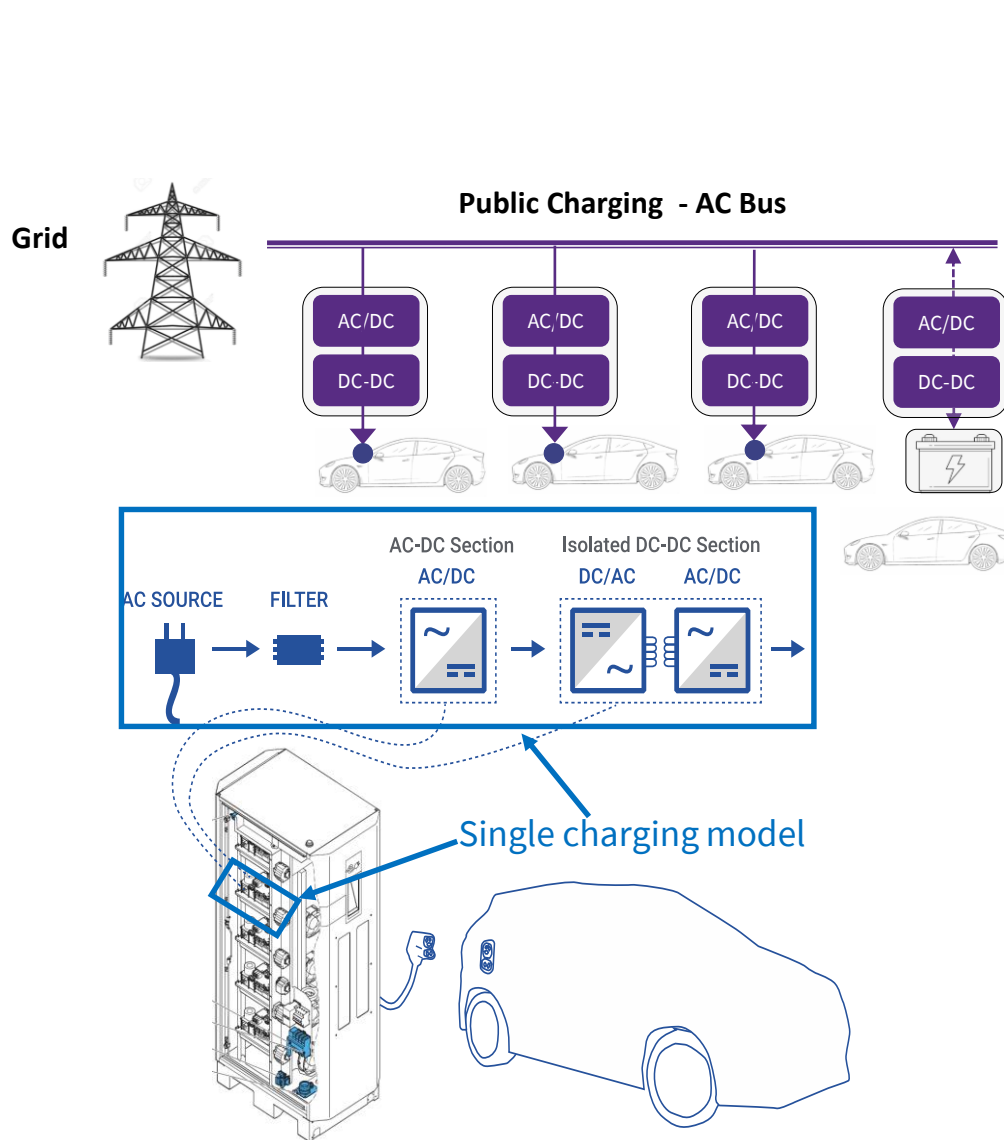
Tesla Model S



Ford Mach-E

- **EV owners:** Resolve mileage anxiety, better charging experience
- **Automakers:** Selling point for mainstream and high-end cars
- **Charging point operators:** Shorter charging time, higher turn over, more cashflow

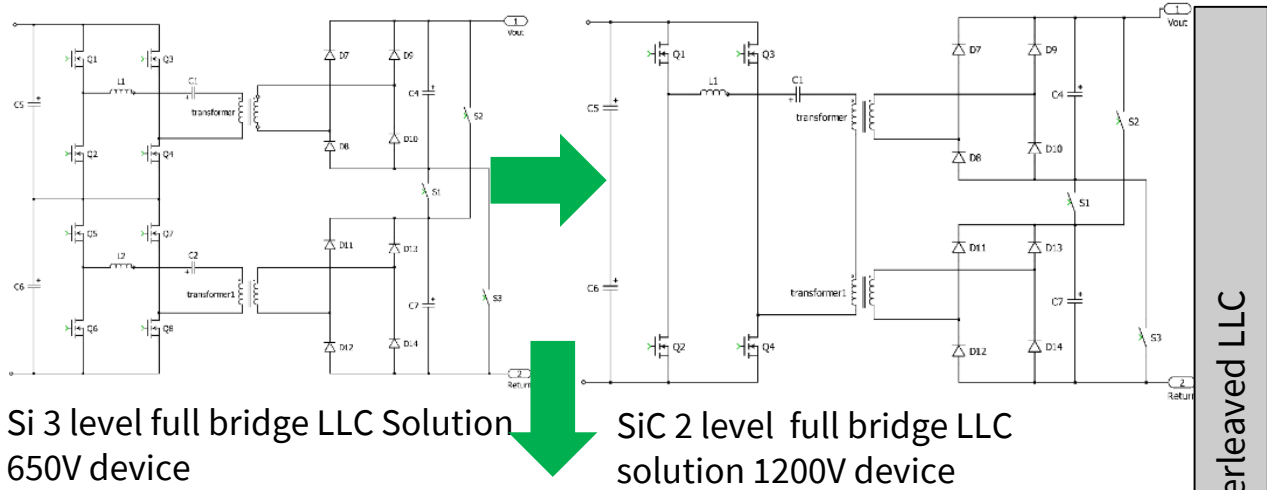
# DC FAST CHARGER – CHALLENGE AND TREND



## Trend

- Very wide output voltage range: 200V-1000V
- High efficiency, high power density and competitive cost
- Increasing power level for each module: 15kW/20kW → 30kW, 40kW and 60kW

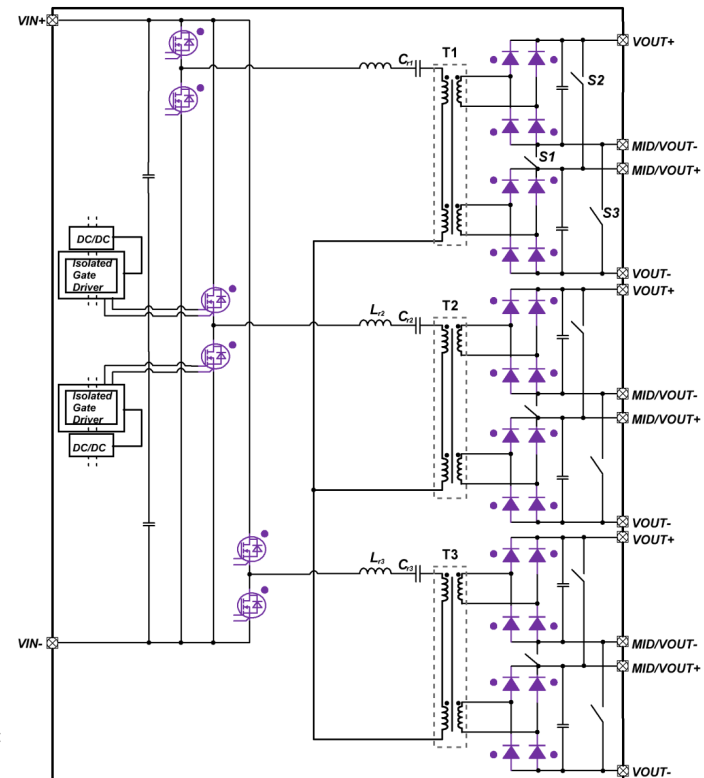
# TOPOLOGY SELECTION



Si 3 level full bridge LLC Solution  
650V device

SiC 2 level full bridge LLC  
solution 1200V device

30k-60kW & above  
SiC 2 level 1200V  
Device, 3 phase  
interleaved LLC

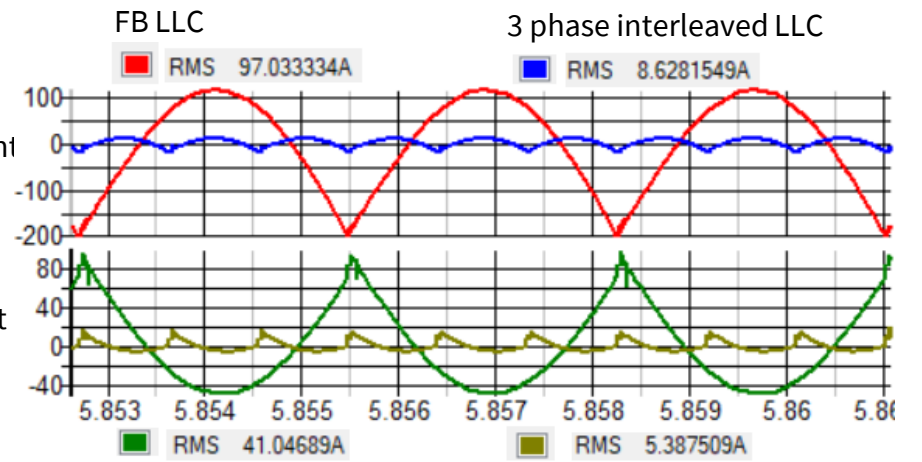


Three-Phase Interleaved LLC

BENEFITS	CHALLENGES
<ul style="list-style-type: none"><li>• <b>Low input current ripple  </b></li><li>• <b>Low output ripple   Smaller output Capacitor</b></li><li>• Uniform distribution of Power to Three Phase on Primary</li><li>• Flexible discrete solution with 1x or 2x SiC FET per position</li></ul>	<ul style="list-style-type: none"><li>• Tolerance of resonant C,L and magnetizing Lm can cause unbalanced currents</li><li>• Complex vector control although three phase analysis applies</li></ul>

Output ripple current  
@300V/200A

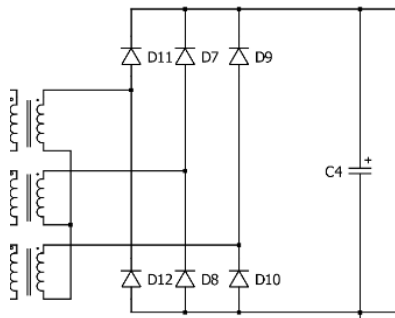
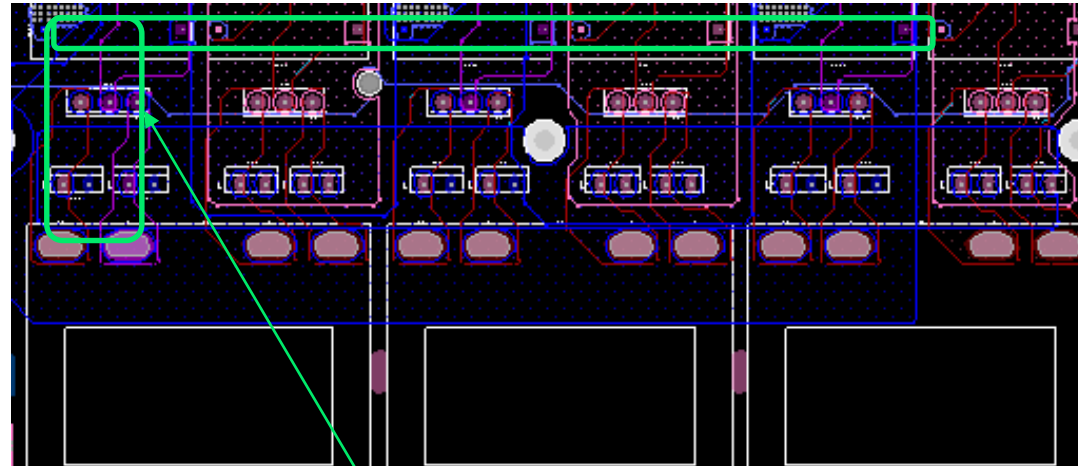
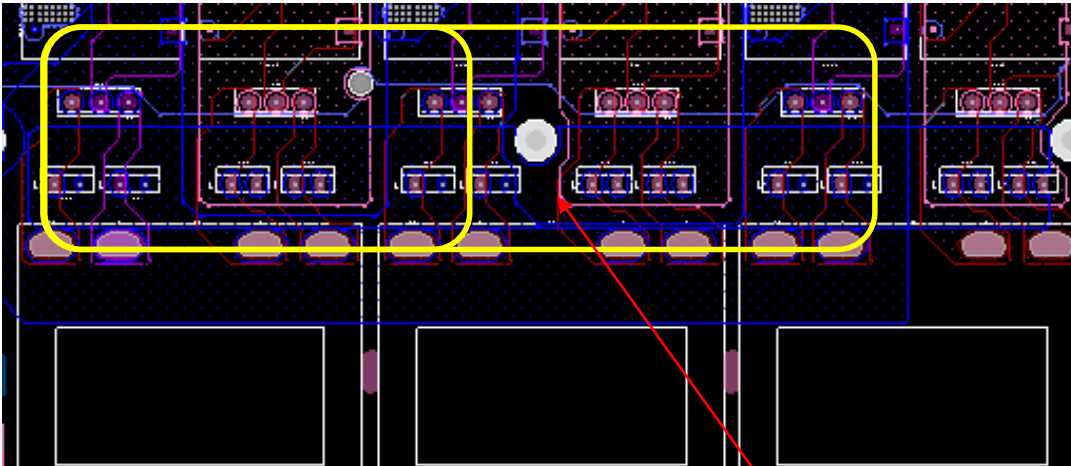
Input ripple current  
@300V/200A



# TOPOLOGY SELECTION

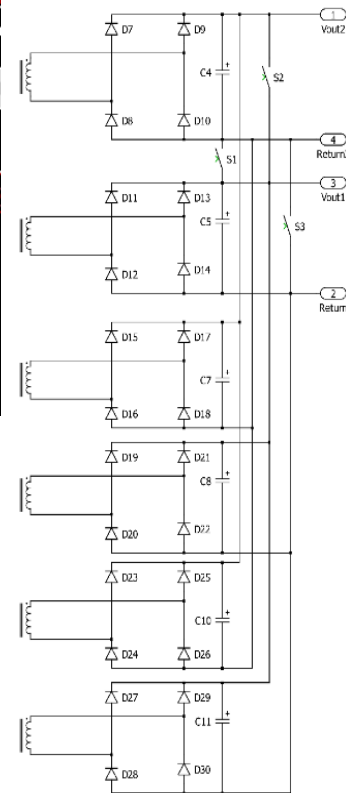
3phase output Bridge rectifier

Full Bridge output rectifier

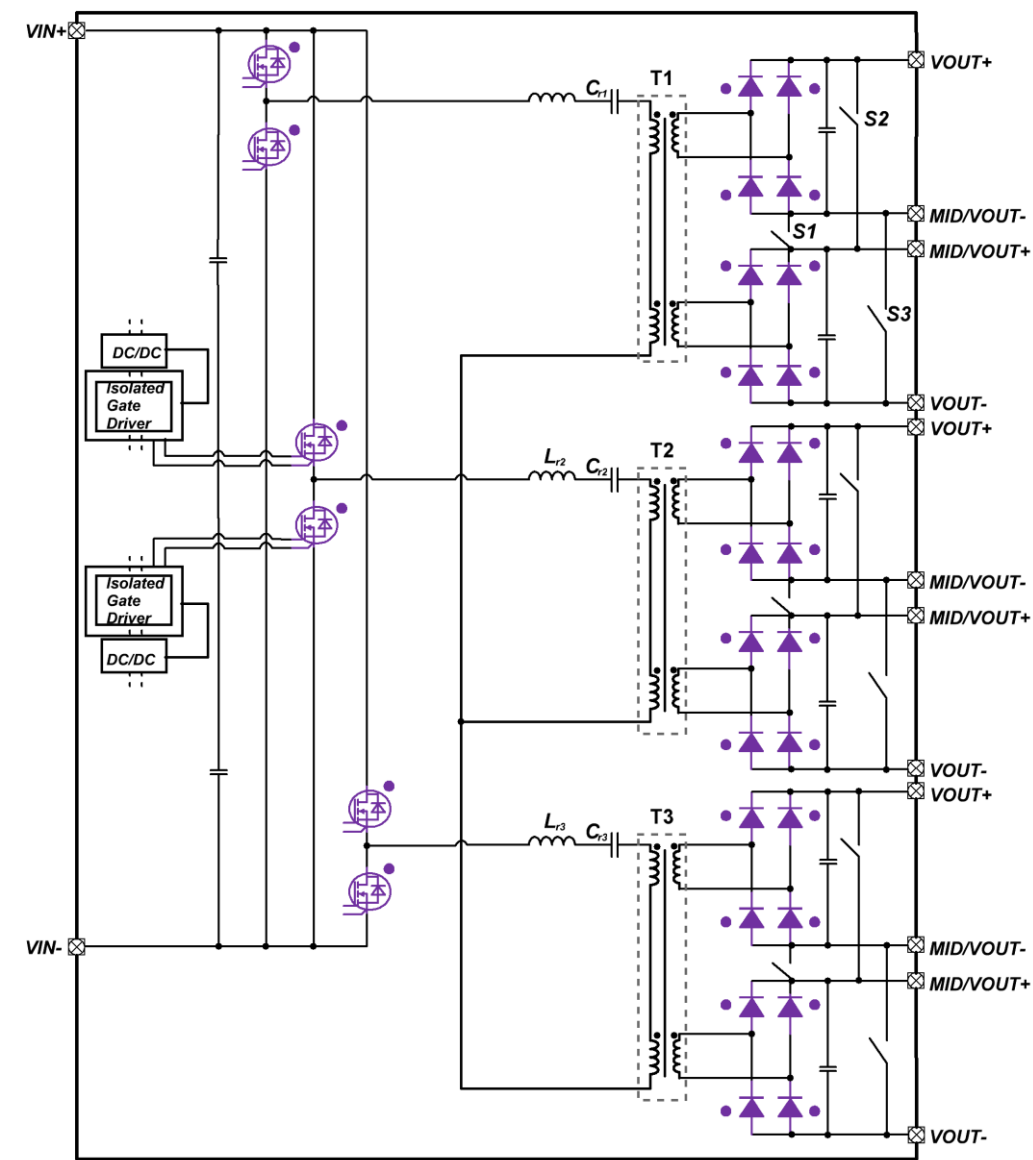


Large loop for  $di/dt$   
Magnetic field  
to input EMI filters

Small loop for  $di/dt$ ,  
more EMI friendly



# QUICK SPEC OF CRD-60DD12N-K

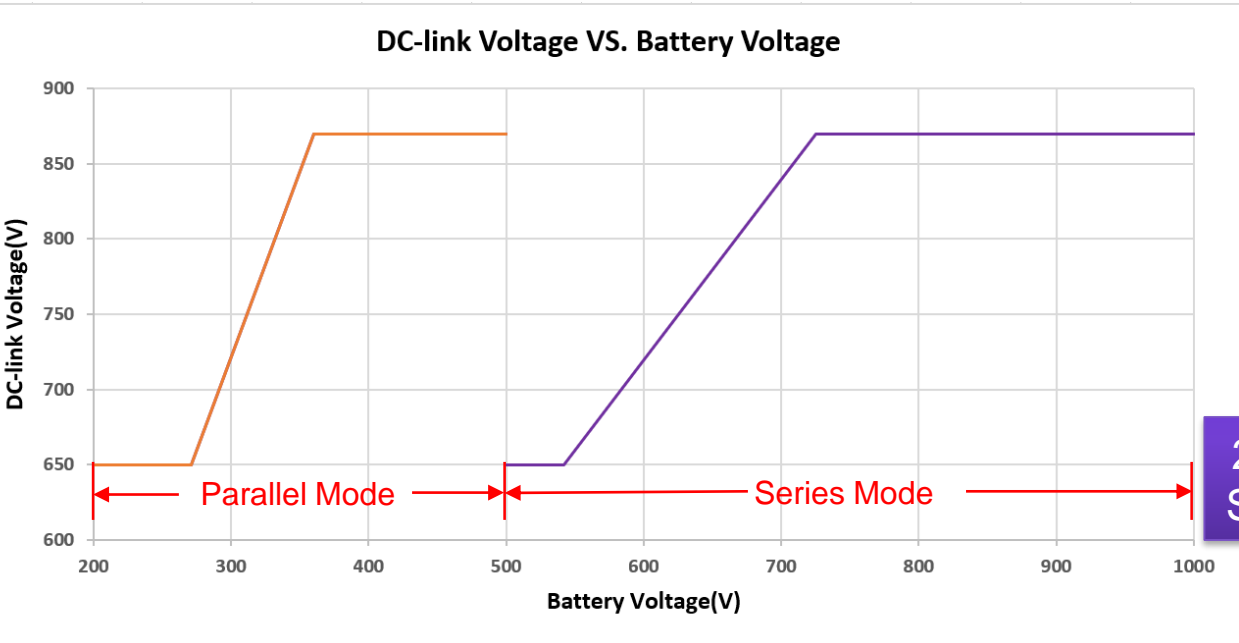


Description	Specifications
DC Input Voltage	650Vdc - 850Vdc
DC output	200V-1000V; CP 60kW when Vo >= 300V
Switching Frequency	Fr=180kHz
PCBA size	490mm*390mm*65mm
Efficiency LLC	>98%(peak), >97%(full load), >96.5%@ Vout=300V
Cooling	Forced air cooling

- 12 discrete SiC MOSFETs deliver 60kw output power
- Three phase interleaved LLC reduce both input and output ripple current
- SiC MOSFETs enables High efficiency and high power density
- Flexible voltage gain control scheme enables wide output voltage range
- Excellence current sharing between paralleled MOSFETs



# CONTROL AND MOSFETS SELECTION



$f_r=180\text{kHz}$   $125\text{k}<f_s<250\text{kHz}$   
 $L_r=7.5\mu\text{H}$   $C_r=102\text{nF}$  (LLC)  
 $L_m=30\mu\text{H}$

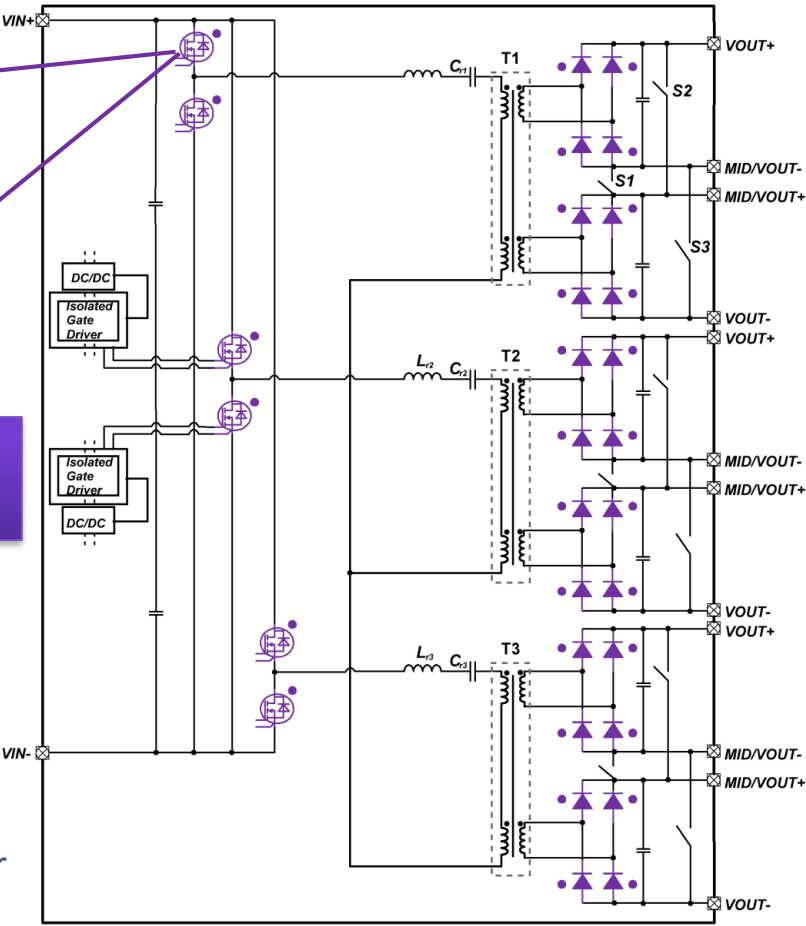


2 PCs 1200V 40 mohm  
SiC MOSFET in parallel

## 60kW design

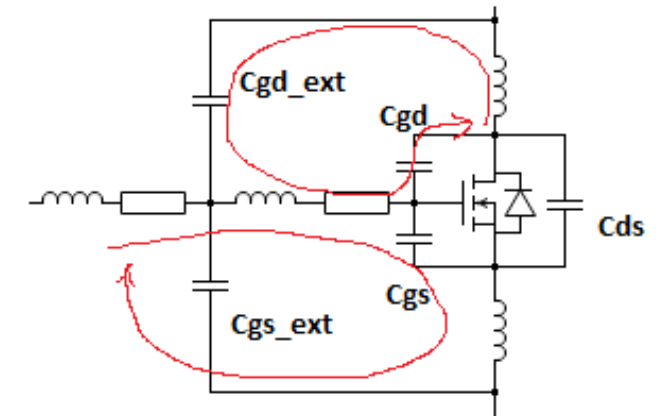
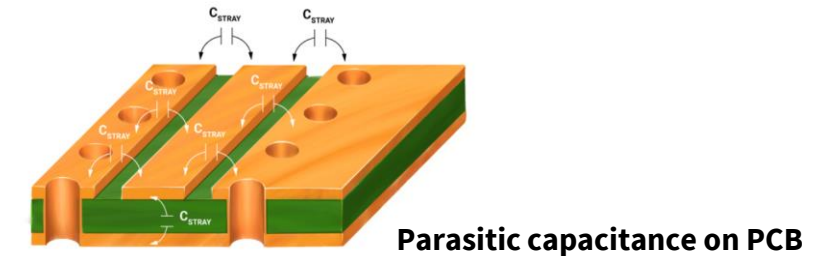
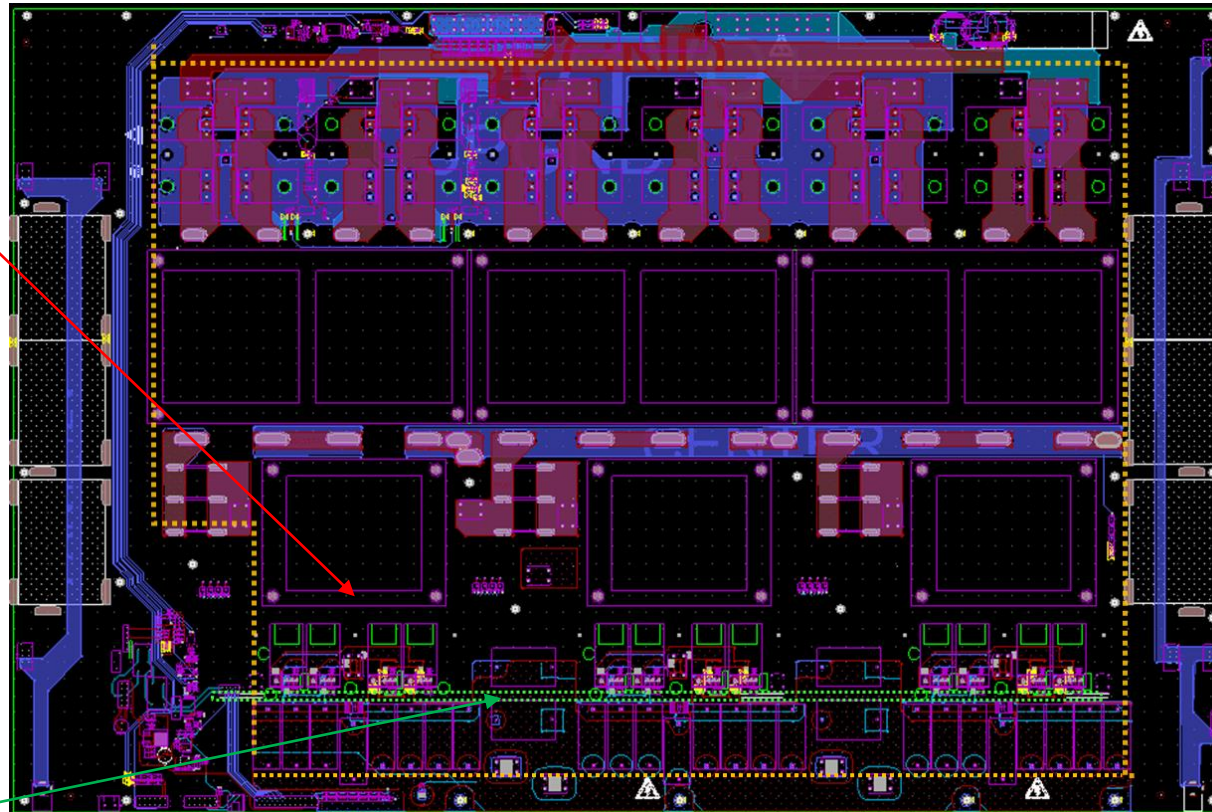
- 12x 1200V 40mOhm SiC

32mohm, 21 mohm for higher  
efficiency



# COMPONENTS PLACEMENT

Similar PCB design rules for SiC and Si → Avoid overlap between Gate+Gate-drive-circuit and the drain of MOSFET.

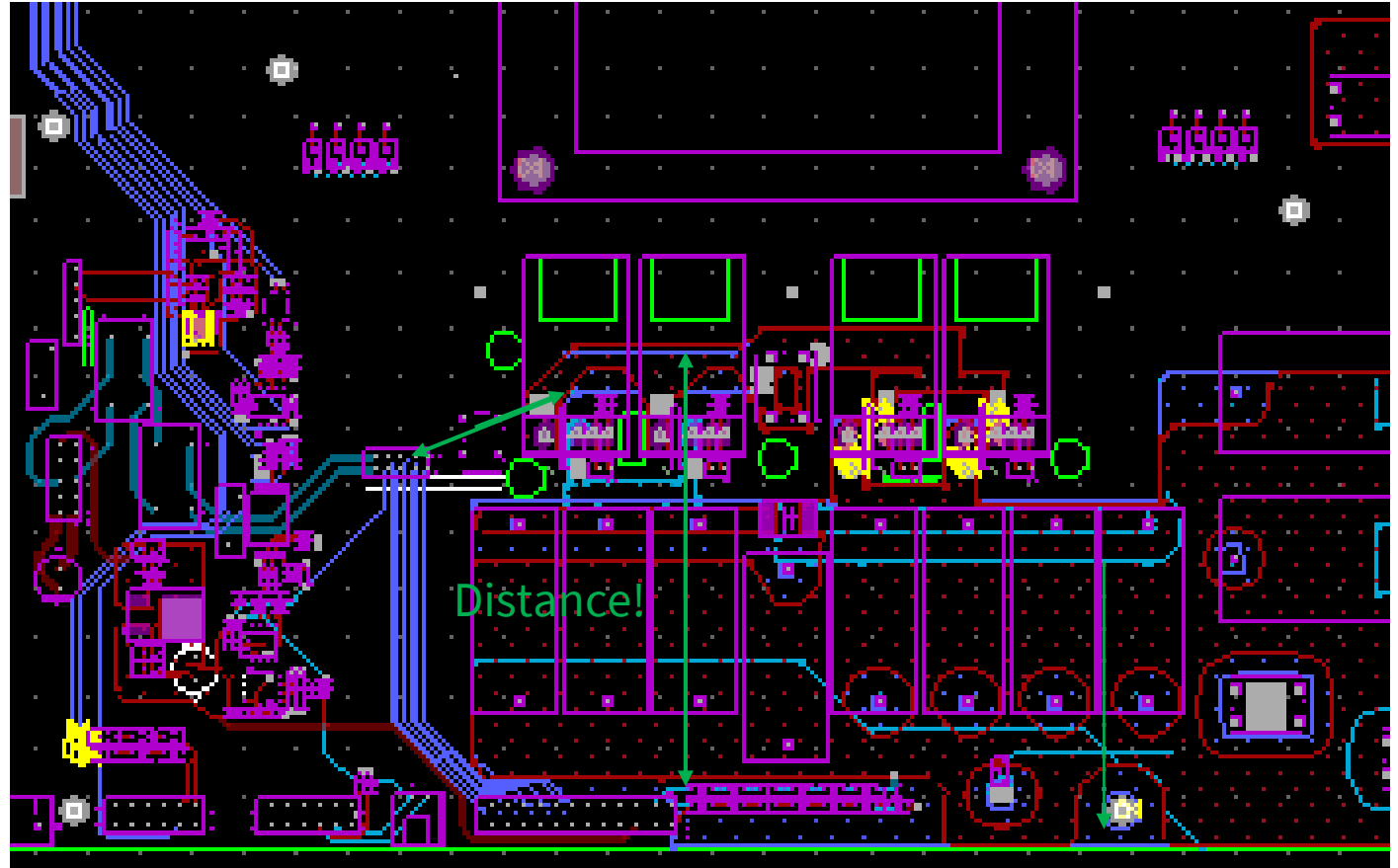
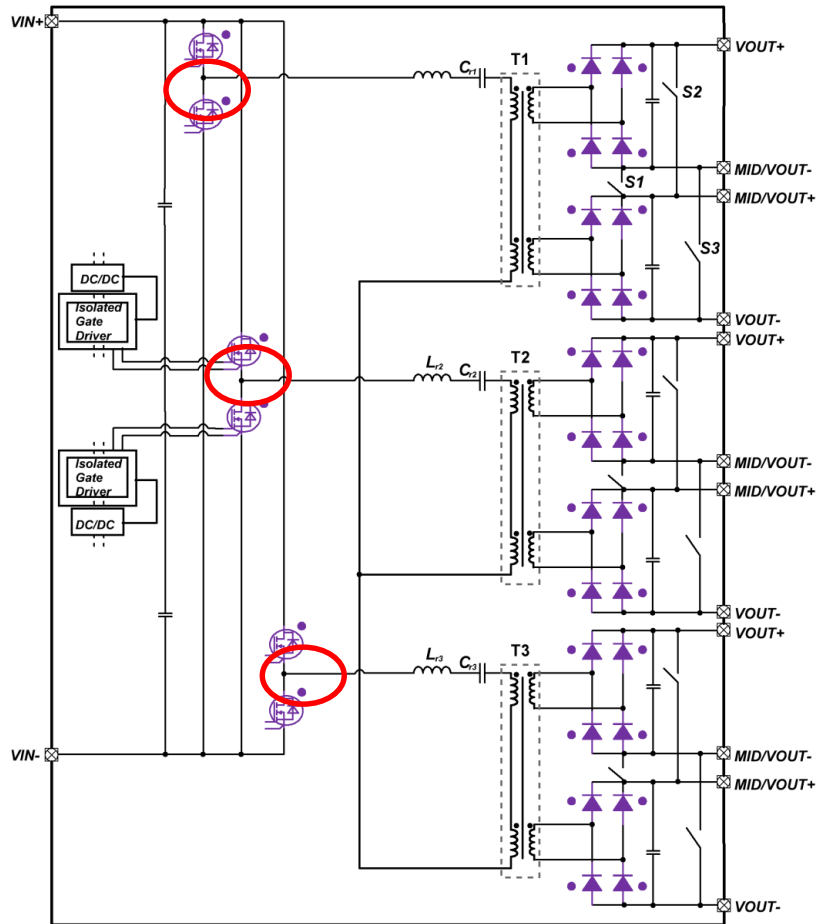


Consequences external  $C_{gd}$ :

- Not only higher switching loss
- Risk of gate oscillation
- EMI

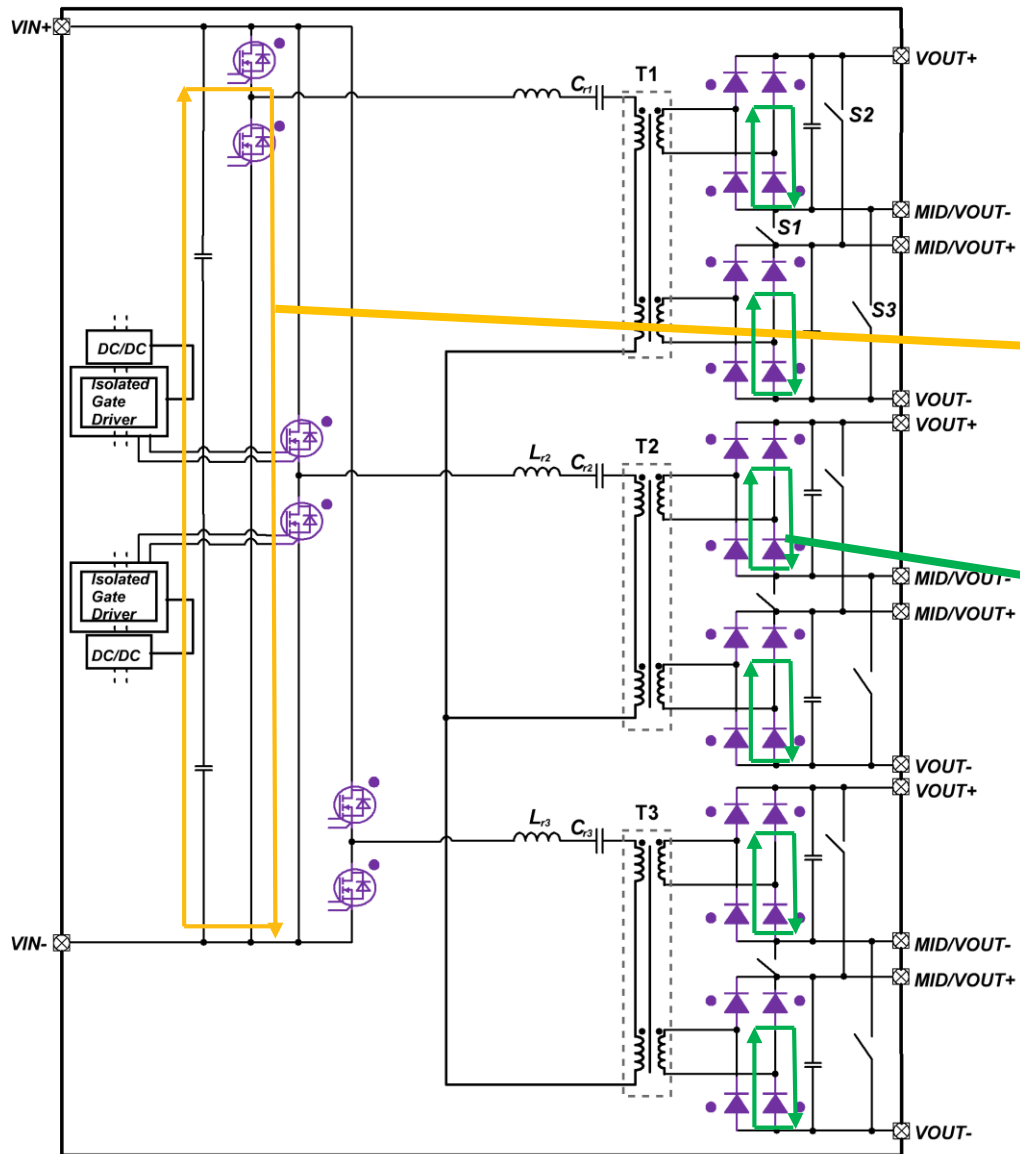


# HIGH DV/DT TRACES/NODES

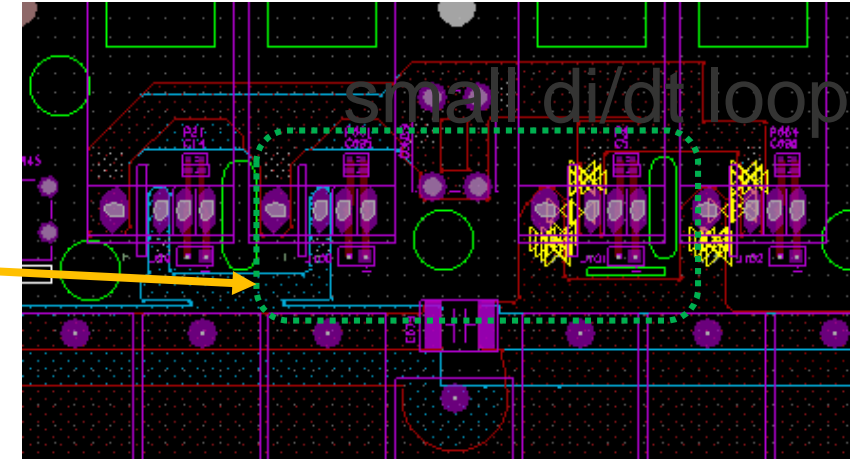


- Keep the sensitive signals(sensing, PWM, communication) far away from the high  $dV/dt$  trace/nodes.
- Keep the sensitive signals far away from the high magnetic field such as resonant choke, power transformer.
- Small pad size of high  $dV/dt$  nodes to reduce the coupling and parasitic capacitance

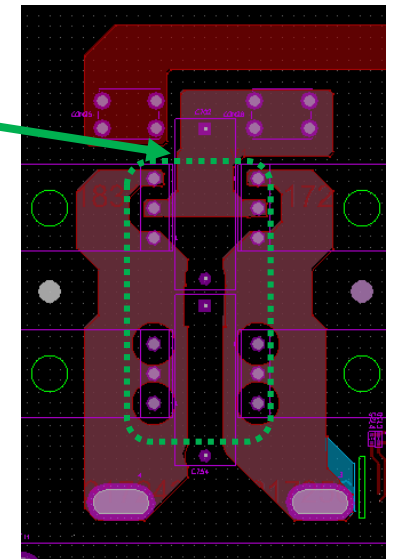
# HIGH DI/DT LOOP



small di/dt loop

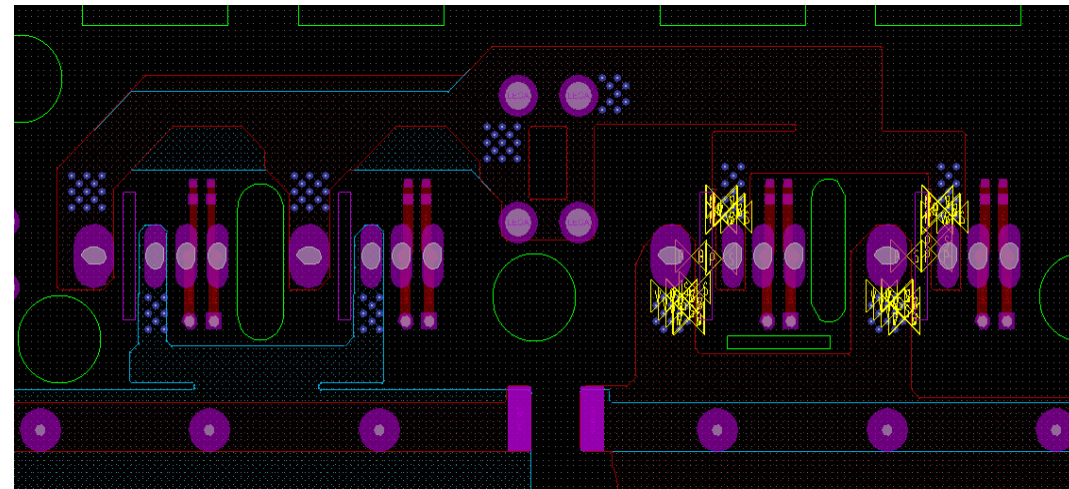
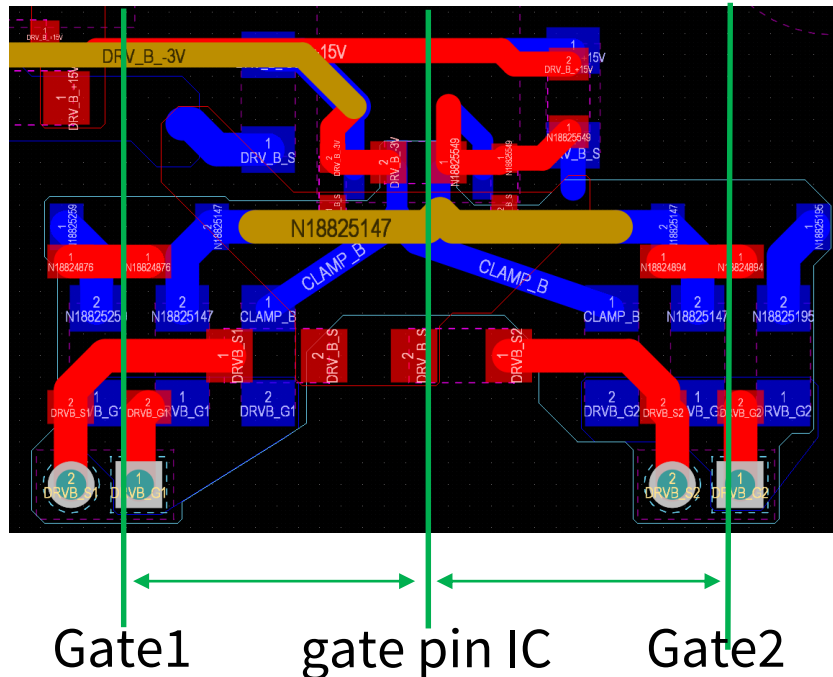
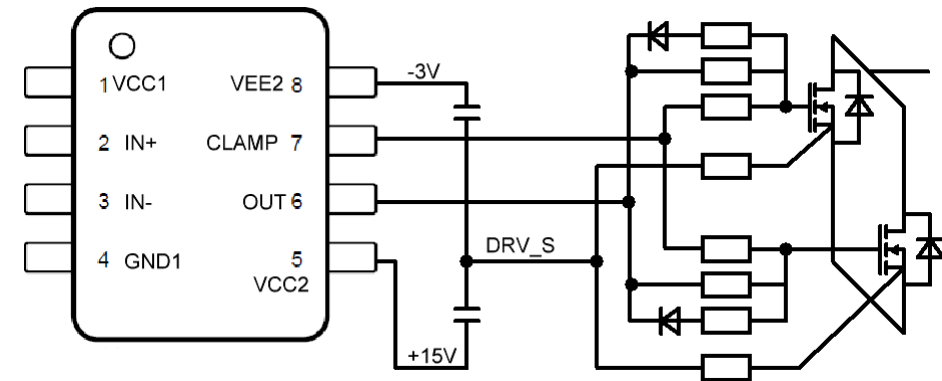


small di/dt loop



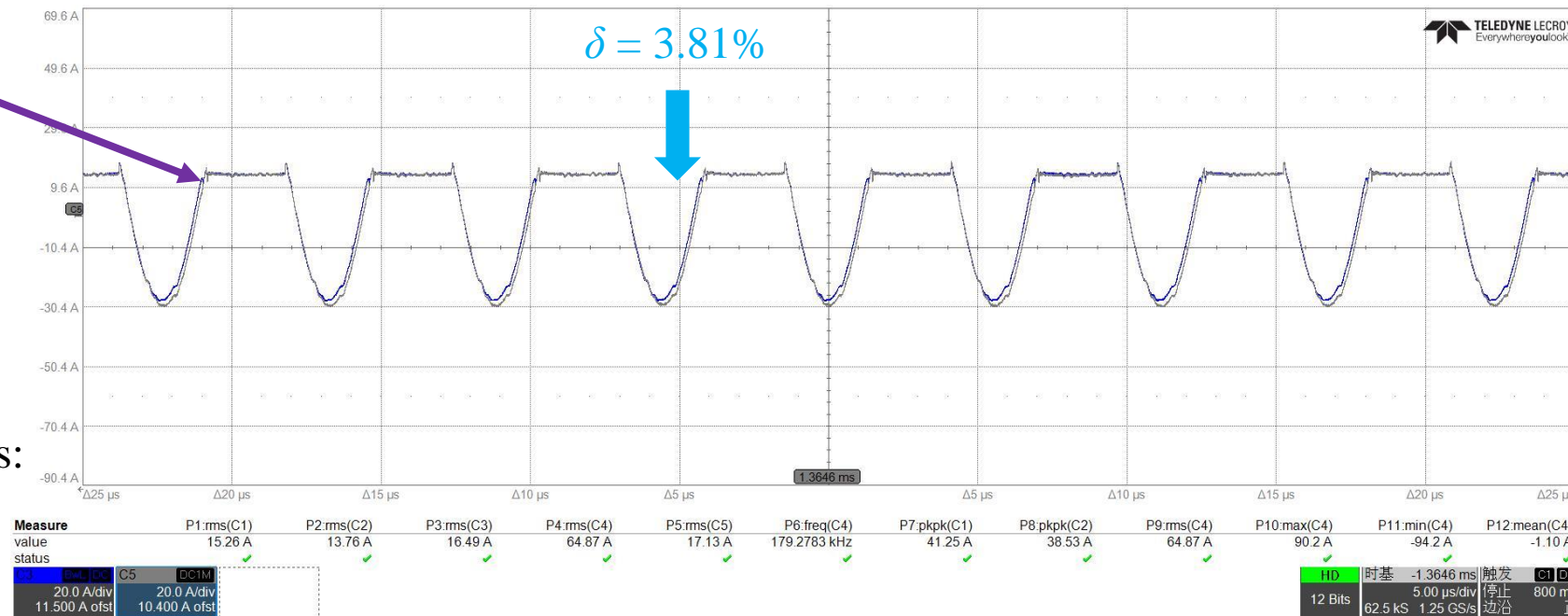
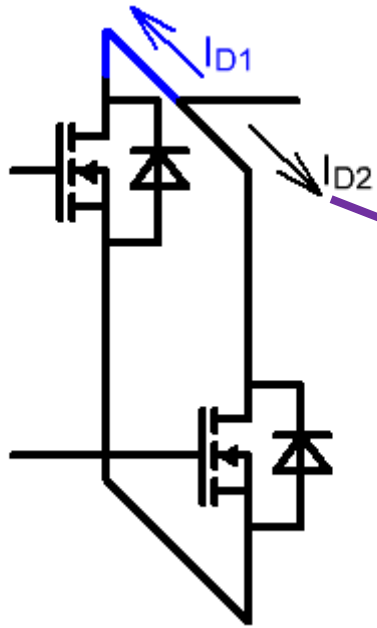
## PCB LAYOUT FOR PARALLELED SIC MOSFET IN 60KW REFERENCE DESIGN

- Minimized the loop of gate drive and active miller clamp
- Symmetrical Gate and return paths
- Have resistors in both Gate and Kelvin-Source and close to the MOSFETs



- Add a small inductance to power source pin of the paralleled MOSFET to improve dynamic current sharing.
- Minimize stray inductance at drain

# CURRENT SHARING BETWEEN PARALLELED MOSFETS



The current unbalance rate  $\delta$  is calculated as:

$$\delta = \frac{\Delta I}{I_{avg}} \times 100\%$$

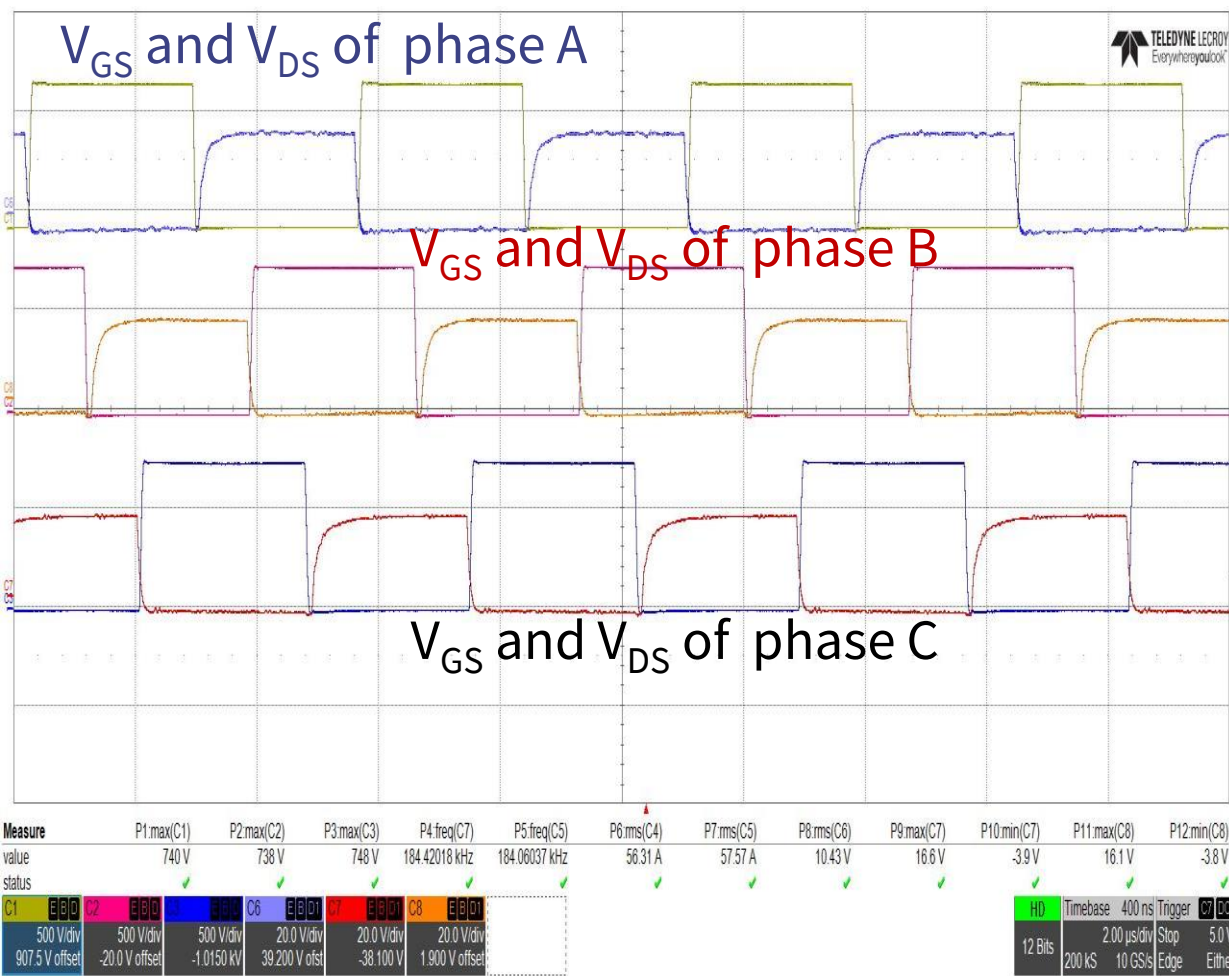
Where:

$\Delta I$  ——— Current difference between the two parallel MOSFETs

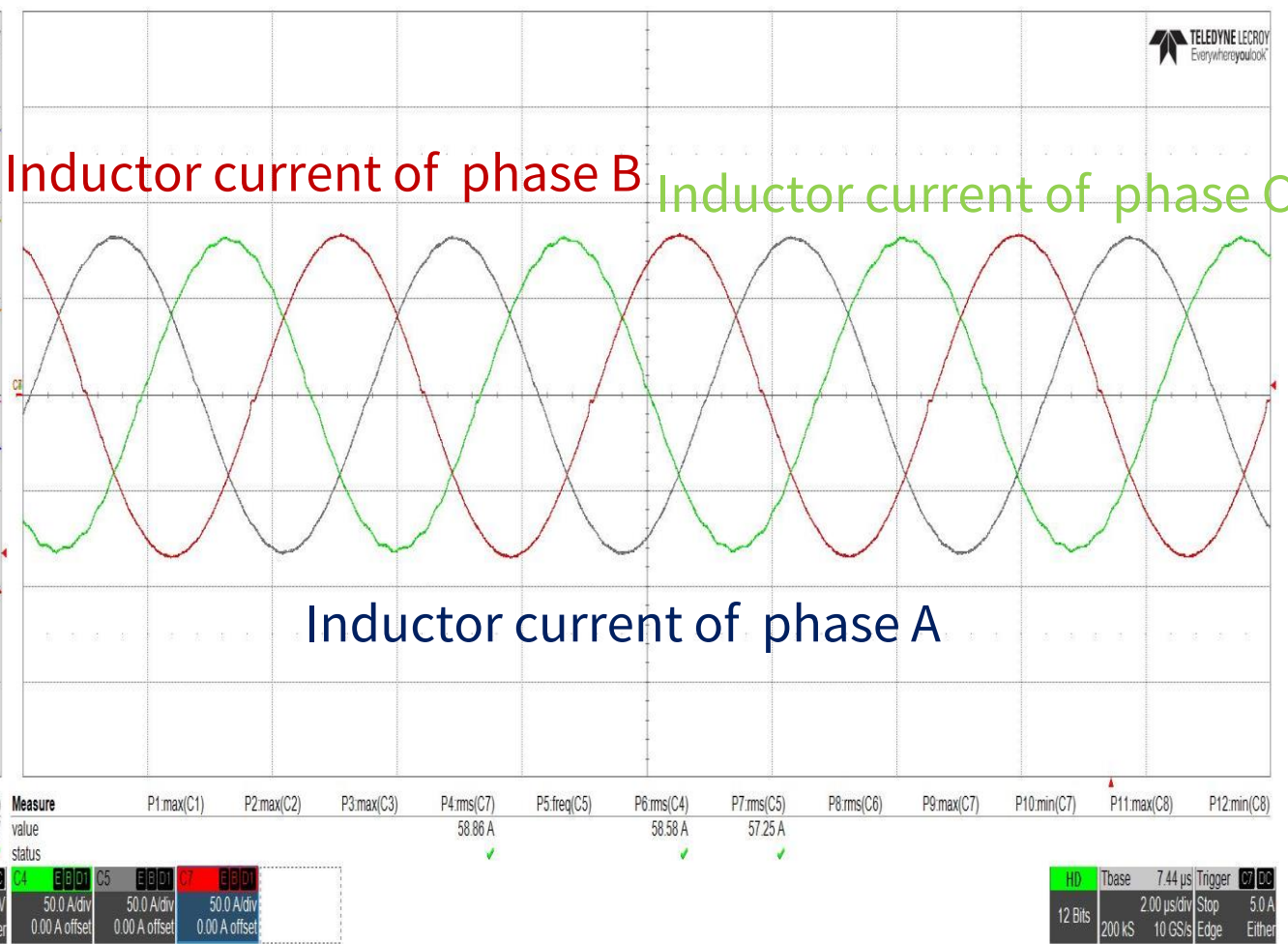
$I_{avg}$  ——— Average current of the two parallel MOSFETs

# WAVEFORMS THREE PHASE INTERLEAVED OPERATION

## ZVS Operation

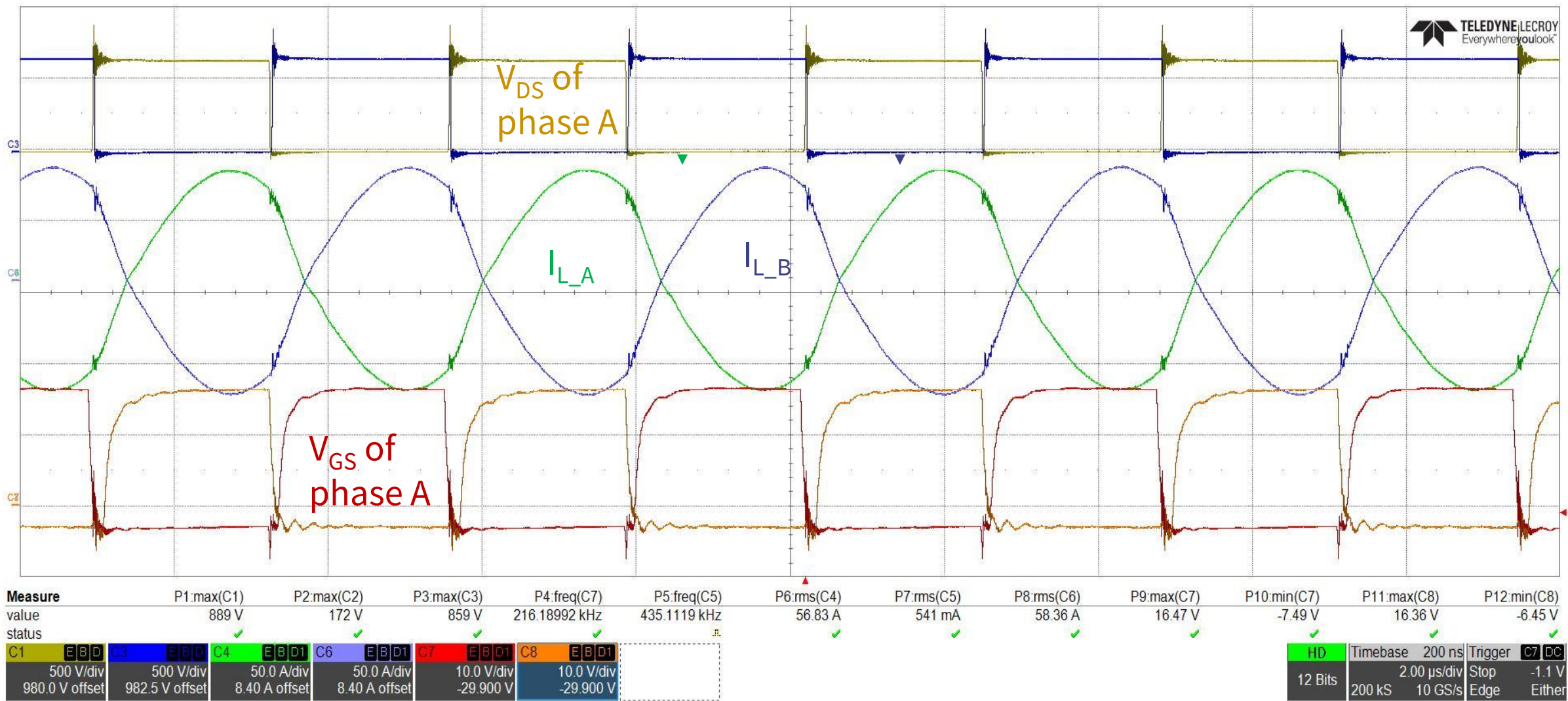


## Balance current in resonant tank

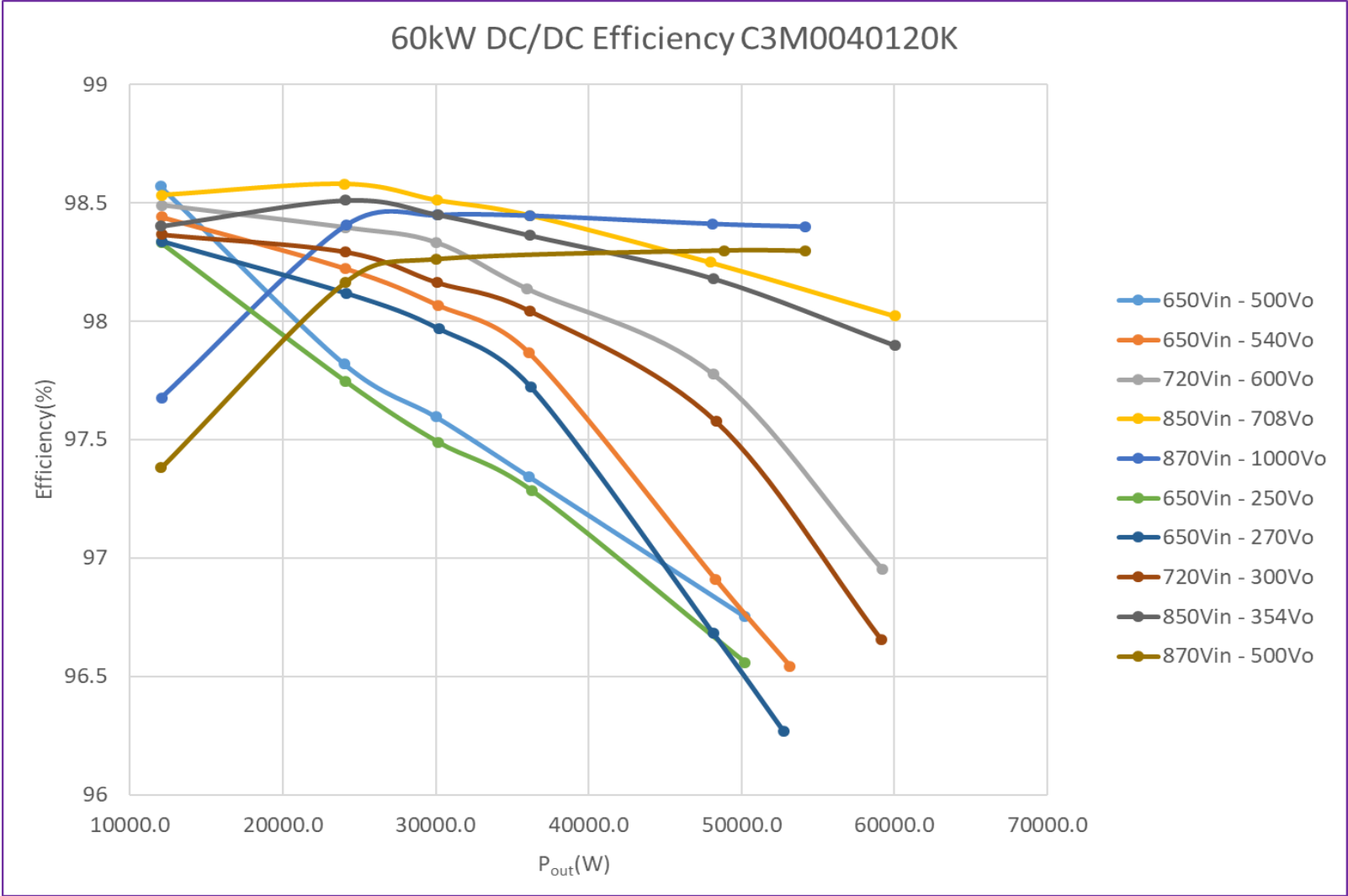




# WAVEFORMS FULL BRIDGE OPERATION (<26KW) FOR LOW OUTPUT VOLTAGE(<250V)



# EFFICIENCY TEST RESULT



## THERMAL RESULTS (TESTED $T_J < MAX T_J * 0.8 = 140\text{ }^{\circ}\text{C}$ )

Part Number	Heatsink Temp.	Rth (j-c) (c/w)	Calculated Power Loss (watts)	Case Temp.	Calculated Junction Temp.	Max. Junction Temp.	Comments
<b>720Vdc Input, 300Vdc Output, full load</b>							
<b>C3M0040120K Q23</b>	85	0.46	33.2	96.6	111.9	175 °C	<b>PASS</b>
<b>650Vdc Input, 200Vdc Output, full bridge mode</b>							
<b>C3M0040120K Q23</b>	85	0.46	47.5	101.6	123.4	175 °C	<b>PASS</b>
<b>870Vdc Input, 500Vdc Output, full load</b>							
<b>C3M0040120K Q23</b>	85	0.46	31	95.8	110.06	175 °C	<b>PASS</b>

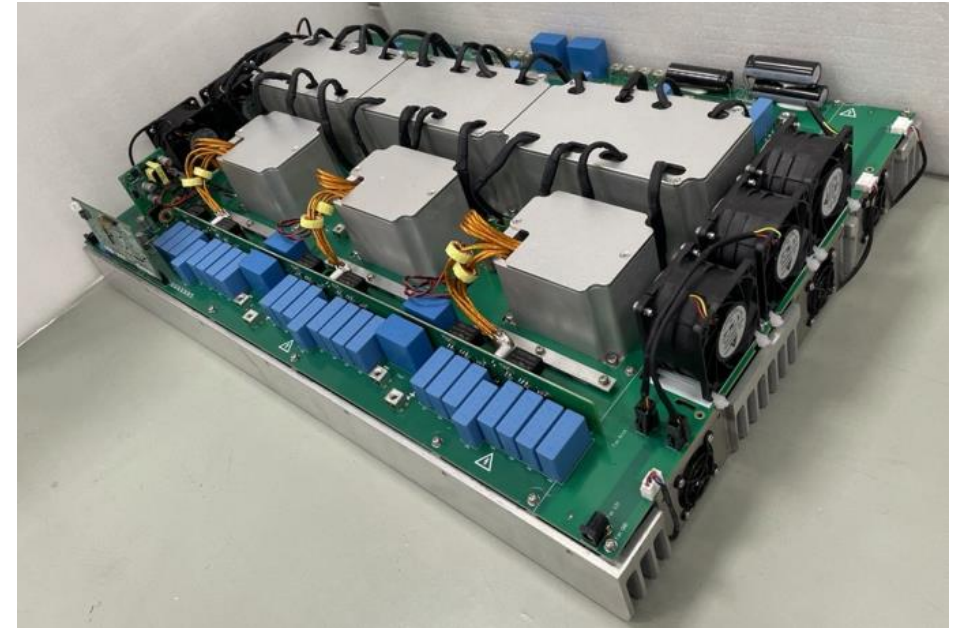
# SUMMARY

The value to get the low power loss from:

- C3M 1200V SiC MOSFET,
- the flexible control scheme
- proper PCB layout

Below design targets are achieved:

- ✓ Low parts counts, 12 pcs TO-247-4 1200V 40mohm SiC discrete MOSFETs to cover 60kW
- ✓ High Efficiency up to 98.5% for DC DC converter
- ✓ Wide battery voltage range 200Vdc-1000Vdc
- ✓ Good Current Sharing between phases and MOSFETs







Thank you!

